FADC board for COT ASDQ analog outputs

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Outline

- COT ASDQ analog outputs
- VME FADC card
- Cost & schedule
- Power
- Draft schematics
COT ASDQ analog outputs

- 1–3 per card available
  (card covers 2 cells, 1260 cards in COT)
- In practice, bring out 12/quadrant = 96 total channels
- We want, in real time, to look at analog outputs with an oscilloscope:
  - debug noise problems
  - measure gain
  - put scope upstairs, use analog mux to reduce cable count
- But we also want to correlate analog outputs with reconstructed tracks:
  - study 2-track resolution
  - map out dE/dx response
  - tune simulation
- Ideally, want a digital scope read out with event data
VME FADC board

- Basically a 6-channel 500Msample/sec scope, designed for CDF DAQ readout
- Need 2 boards/quadrant; would live in TDC crates
- Board has six copies of
  - differential receiver/amplifier (×1 ~ ×10 gain)
    * input: [−50, 50] ~ [−500, 500]mV
    * Maxim 4145 output: [−500, 500]mV
    * second stage (AD8037) ⇒ [−2, 0]V for FADC
  - SPT 7750 FADC
    * 8 bits/sample at 500 MS/s
    * double buffered to 16 bits at 250 MHz
    * ECL output
  - ECL→TTL latches
    * buffer down to 32 bits at 125 MHz, which FPGA can handle comfortably
  - Altera APEX 20K100E FPGA, 356-pin BGA
    * ~100K gates, 52Kbits RAM (5.5μs ~ 22Kbits)
    * 246 I/O pins, 4 clock input pins, up to 250MHz
    * 1.8V VCC for logic, 3.3V for TTL-compatible I/O
    * successor of Flex 10K family used in trigger boards
- Oscillator: Connor-Winfield GA01-541, 495.8 MHz (in stock), ECL, DIP-16, in principle swappable
More facts & features

- FADC outputs are valid for 2.5ns out of 4ns period; plenty of time for ECL latches
- Firmware-programmable sampling window, nominally 256 nsec (128 samples), delayed 0–8192 ns for L1A
- Not a problem for sampling window to be wider than CDF clock period (tested in Altera simulation)
- Implement standard 42-crossing L1 pipeline as circular memory buffer in FPGA internal dual-ported SRAM
- 4-buffer CDF standard VME readout
- Possibly on-board zero suppression
- Copy VME interface from Chicago trigger boards
- Uncompressed data size: \( \frac{256 \text{ nsec}}{2 \text{ nsec/sample}} \times \frac{1 \text{ byte}}{\text{sample}} \times \frac{6 \text{ channels}}{\text{board}} \times 16 \text{ boards} = 12 \text{ KB/event} \)
- Readout time: \( \frac{2 \text{ boards}}{\text{crate}} \times \frac{768 \text{ bytes}}{\text{board}} \times \frac{\sim 300 \text{ nsec}}{4 \text{ bytes}} \approx 100 \mu\text{sec} \)
- External trigger input (TTL, 50 \( \Omega \)) for standalone mode
- Bandwidth \( \sim 100 \text{ MHz @ } \times 10 \text{ gain} \)
- 4145 allows pole-zero correction (for cable loss) without affecting input termination
- Calibration plan TBD (inject current at input terminator)
- 2 nsec sampling is the fastest we’re able to do with the parts we know how to use
- 2 nsec looks fine for COT pulses
- note TDC time bin is 1 nsec
Analog repeater schematic

Channels to be monitored

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![Image of analog repeater schematic]

![Image of channels to be monitored]
~1.5 mV noise
~15 mV step signal

Analog repeater

Maxim 4445

FADC card

\( x \times 10 \approx 200 \text{ mV/Div} \)

\( \pm 250 \text{ mV range} \)

300 \( \approx 100 \text{ MHz} \)

\( \approx 2.4 \times 10^7 \)

\( 5 \times 10^7 \)

\( 20 \text{ Ohm} \)

10\(^{-1}\) - 90\(^{-1}\). Rise \( \leq 3 \text{ nsec} \)
Cost & schedule

- Estimate $10–15K for parts, PCB, & assembly of 2 prototypes
- Per-board parts cost $3K:
  - $100–150
  - $300–350
  - $25
  - Connor-Winfield 495.8 MHz ECL osc, $50
- ~ 3 months engineering effort
- Order prototype parts in next few days
- Probably ready ~ November
  (ideally, optimistically, before end of C-run)
- Build full set of 16 boards (+ spares) by March, probably $4–5K/board
Power

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- Total board power $\sim$ 100 W